Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-15. (Canceled)

16. (Currently amended) A method of manufacturing a semiconductor device comprising:

a preparation step including:

preliminarily forming on a sample wafer a test pattern having three-dimensional line and space patterns and an actual circuit pattern having three dimensional portions while varying a process parameter in the semiconductor manufacturing process used to make the sample wafer;

~~using an optical scatterometry apparatus,~~ measuring a feature of the test pattern using an optical scatterometry apparatus; ~~and~~

measuring a feature of a ~~critical~~ predetermined portion of the actual circuit pattern using a three-dimensional measuring apparatus; and

calculating a first correspondence relationship between the feature of the test pattern and the feature of the actual circuit pattern, and a second correspondence relationship between the process parameter and the measured features; and

an evaluation step including:

measuring a feature of ~~the~~ a test pattern formed on a manufactured wafer on a semiconductor process line by use of the optical scatterometry apparatus;

determining a process parameter based on the ~~first~~ second correspondence relationship;

estimating ~~an amount of the critical~~ a measurement of a predetermined portion of an actual circuit pattern formed on the manufactured wafer based on the ~~second~~ first correspondence relationship; and

evaluating the semiconductor manufacturing process line for the actual circuit pattern based on the estimated measurement~~amount~~.

17. (Canceled)

18. (Previously presented) A method as in claim 16 wherein in the preparation step and the evaluation step the semiconductor manufacturing process comprises a semiconductor exposure and development step, and the process parameter includes at least one of exposure and focus.

19. (Previously presented) A method as in claim 16 wherein in the preparation step and the evaluation step, the semiconductor manufacturing process includes a semiconductor etching process, and the process parameter comprises at least one of gas flow rate, pressure variation, and etching time.

20. (Previously presented) A method as in claim 16 wherein the evaluation step includes a step of displaying the process parameter on a process window as a range of process parameters with a plurality of circuit patterns, and the process window is determined based upon the second correspondence relationship.

21-26. (Canceled)